CLAIMS:

1. A multistage bit stream multiplexer having a switchable forward/reverse clock relationship comprising:

a first multiplexing integrated circuit that receives a first plurality of bit streams at a first bit rate and that produces a second plurality of bit streams at a second bit rate, wherein the first plurality of bit streams are greater in number than the second plurality of bit streams are in number, and wherein the first bit rate is less than the second bit rate;

a second multiplexing integrated circuit that receives the second plurality of bit streams and that outputs at least one high-speed bit stream at a line bit rate that exceeds the second bit rate; and

a clock circuit, wherein the clock circuit generates a forward transmit clock for use by the first multiplexing integrated circuit in producing the second plurality of bit streams based upon a reference clock signal selectable from a plurality of inputs, wherein the inputs include a reverse transmit clock generated by the second multiplexing integrated circuit.

2. The multistage bit stream multiplexer of Claim 1, further comprising:

a communication Application Specific Integrated Circuit (ASIC) from which the first multiplexing integrated circuit receives the first plurality of bit streams; and

a media interface that receives the at least one high-speed bit stream and produces a media output.

3. The multistage bit stream multiplexer of Claim 1, wherein the plurality of inputs further comprises an external oscillator output.

4. The multistage bit stream multiplexer of Claim 1, wherein the plurality of inputs further comprises a voltage controlled oscillator output.

5. The multistage bit stream multiplexer of Claim 1, wherein the reference clock signal is selected based upon a clock selector input .

6. The multistage bit stream multiplexer of Claim 5, wherein the first multiplexing integrated circuit further comprises a phase locked loop (PLL) that receives the reference clock signal and produces a PLL Data Clock having a frequency equal to the second bit rate, and wherein a plurality of latches receive the PLL Data Clock, latch data multiplexed from the first plurality of bit streams and produce the second plurality of bit streams.

7. The multistage bit stream multiplexer of Claim 6, wherein the frequency of the PLL Data Clock is 16 times the frequency of the reference clock

8. The multistage bit stream multiplexer of Claim 7, further comprising a division circuit that receives the PLL Data Clock and generates an output used to produce the forward transmit clock.

9. The multistage bit stream multiplexer of Claim 1, wherein the forward transmit clock is a source centered double data rate clock with respect to each of the plurality of second bit streams.

10. The multistage bit stream multiplexer of Claim 6, wherein the PLL outputs to the second multiplexing integrated circuit, a lock detect signal that remains active while the PLL is locked to the reference clock signal and becomes inactive when the PLL is not locked to the reference clock signal, and wherein the first multiplexing integrated circuit selects the reverse clock through the clock selector when the PLL is not locked to the reference clock signal.

11. The multistage bit stream multiplexer of Claim 1, wherein the first multiplexing integrated circuit generates the reverse clock based on an external oscillator reference clock.

12. The multistage bit stream multiplexer of Claim 4, wherein the first multiplexing integrated circuit further comprises a phase detector that receives a first input from a loop timing circuit and a second input from one of the plurality on inputs.

13. The multistage bit stream multiplexer of Claim 1, wherein the first multiplexing integrated circuit comprises integrated circuits formed on a silicon substrate and the second multiplexing integrated circuit comprises a substrate selected from the group consisting of InP, SiGe, GaN, GaAs, and Si.

14. An upstream multiplexing integrated circuit within a multi-stage bit stream multiplexer that operates with a switchable forward/reverse lock relationship with an downstream multiplexing integrated circuit, comprising:

a plurality of input ports operable to receive a first plurality of bit streams at a first bit rate;

a plurality of output ports to output a second plurality of bit streams at a second bit rate, wherein the first plurality of bit streams is greater in number than the second plurality of bit streams are in number, and wherein the first bit rate is less than the second bit rate; and

a clock circuit, that generates a forward transmit clock signal for use by the upstream multiplexing integrated circuit in producing the second plurality of bit streams based upon a reference clock signal selectable from a plurality of inputs, wherein said inputs including a reverse transmit generated by the downstream integrated circuit.

15. The upstream multiplexing integrated circuit of Claim 14, wherein the first plurality of bit streams are received from a communication Application Specific Integrated Circuit (ASIC) from which the first multiplexing integrated circuit receives the first plurality of bit streams, and wherein the downstream multiplexing integrated circuit outputs at least one high-speed bit stream to a media interface that produces a media output.

16. The upstream multiplexing integrated circuit of Claim 14, wherein the plurality of inputs further comprises an external oscillator output.

17. The upstream multiplexing integrated circuit of Claim 14, wherein the plurality of inputs further comprises a voltage-controlled oscillator.

18. The upstream multiplexing integrated circuit of Claim 14, wherein the reference clock signal is selected based upon a clock selector input.

19. The upstream multiplexing integrated circuit of Claim 13, further comprising a phase locked loop (PLL) that receives the reference clock signal and produces a PLL Data Clock having a frequency equal to the second bit rate, wherein a plurality of latches receive the PLL Data Clock, latch data multiplexed from the first bit streams and produce the plurality of second bit streams.

20. The upstream multiplexing integrated circuit of Claim 19, wherein the frequency of the PLL Data Clock comprises 16 times the frequency of the reference clock.

21. The upstream multiplexing integrated circuit of Claim 19, further comprising a division circuit that receives the PLL Data Clock and generates an output used to produce the forward transmit clock.

22. The upstream multiplexing integrated circuit of Claim 14, wherein the forward transmit clock is a source centered double data rate clock with respect to the second plurality of bit streams.

23. The upstream multiplexing integrated circuit of Claim 19, wherein the PLL outputs to the upstream multiplexing integrated circuit, a lock detect signal that remains active while the PLL is locked to the reference clock signal and becomes inactive when the PLL is not locked to the reference clock signal, and wherein the downstream multiplexing integrated circuit selects the reverse clock through the clock selector when the PLL is not locked to the reference clock.

24. The upstream multiplexing integrated circuit of Claim 14, wherein the reverse clock is based on an external oscillator reference clock.

25. The upstream multiplexing integrated circuit of Claim 19, further comprising a phase detector that receives a first input from a loop clock and a second input from the voltage controlled oscillator.

26. The upstream multiplexing integrated circuit of Claim 13, further comprising a Si substrate, and wherein the downstream multiplexing integrated circuit comprises a substrate selected from the group consisting of InP, SiGe, GaN, GaAs, and Si and wherein the second multiplexing integrated circuit comprises integrated circuits formed on a Si substrate.

27. A method of multiplexing a first plurality of bit streams to at least one high-speed bit stream with a multistage multiplexer, comprising the steps of:

receiving the first plurality of bit streams at a first stage multiplexing integrated circuit at a first bit rate;

multiplexing the first plurality of bit stream into a second plurality of bit streams at a second bit rate, wherein the second bit rate exceeds the first bit rate;

receiving the second plurality of bit streams at a second stage multiplexing integrated circuit at a second bit rate, wherein the second plurality of bit streams are fewer in number than the first plurality of bit streams is in number;

multiplexing the second plurality of bit stream into at least one high-speed bit streams having a line bit rate that exceeds the second bit rate; and

generating a forward transmit clock from a reference clock signal selectable from a plurality of inputs, wherein the plurality of inputs comprise a reverse transmit clock generated by the second stage multiplexing integrated circuit.

28. The method of Claim 27 wherein further comprising the step of producing a lock detect signal to indicate when a PLL is locked to the reference clock signal, wherein a reverse transmit clock is selected as the reference clock signal when the PLL is not locked to the reference clock.

29. The method of Claim 27, wherein the first plurality of bit streams are received from a communication Application Specific Integrated Circuit (ASIC), and wherein the second stage multiplexing integrated circuit outputs at least one high-speed bit stream to a media interface that produces a media output.

30. The method of Claim 27, wherein the plurality of inputs comprises an external oscillator output.

31. The method of Claim 27, wherein the plurality of inputs further comprises a voltage-controlled oscillator.

32. The method of Claim 27, further comprising the step of selecting the reference clock signal with a clock selector.

33. The method of Claim 27, further comprising the step of receiving the reference clock signal and producing a PLL Data Clock having a frequency equal to the second bit rate with a PLL, wherein a plurality of latches receive the PLL Data Clock, latch multiplexed data from the first bit streams and produce the plurality of second bit streams.

34. The method of Claim 33, wherein the frequency of PLL Data Clock is 16 times the frequency of the reference clock signal.

35. The method of Claim 33, further comprising a division circuit that receives the PLL Data Clock and generates an output used to produce the forward transmit clock.

36. The method of Claim 33, wherein the forward transmit clock is a source centered double data rate clock with respect to the second plurality of bit streams.

37. The method of Claim 33, further comprising the steps of:

generating a lock detect signal that remains active while the PLL is locked to the reference clock signal and becomes inactive when the PLL is not locked to the reference clock signal; and

selecting the reverse clock as the reference clock signal through the clock selector when the PLL is not locked to the reference clock signal.

38. The method of Claim 27, wherein the reverse clock is based on an external oscillator reference clock.

39. The method of Claim 33, further comprising a phase detector that receives a first input from a loop clock and a second input from the voltage controlled oscillator.

40. The method of Claim 33, further comprising a Si substrate, and wherein the downstream multiplexing integrated circuit comprises a substrate selected from the group consisting of InP, SiGe, GaN, GaAs, and Si and wherein the second multiplexing integrated circuit comprises integrated circuits formed on a Si substrate.

41. A method of multiplexing a first plurality of bit streams to at least one high-speed bit stream with a multistage multiplexer, comprising the steps of:

receiving the first plurality of bit streams at a first stage multiplexing integrated circuit at a first bit rate;

multiplexing the first plurality of bit stream into a second plurality of bit streams at a second bit rate;

receiving the second plurality of bit streams at a second stage multiplexing integrated circuit at a second bit rate, wherein the second plurality of bit streams are fewer in number than the first plurality of bit streams are in number, and wherein the first bit rate is less than the second bit rate;

multiplexing the second plurality of bit stream into the at least one high-speed bit streams at a line bit rate that exceeds the second bit rate; and

generating a forward transmit clock from a reference clock signal selectable from a plurality of inputs, wherein the plurality of inputs comprise a reverse transmit clock generated by the second stage multiplexing integrated circuit.

42. The method of Claim 25 wherein further comprising the step of producing a lock detect signal to indicate when a PLL is locked to the reference clock signal, wherein a reverse transmit clock is selected as the reference clock signal when the PLL is not locked to the reference clock.